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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,293	10/27/2003	David C. McClure	03-C-009	3950

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	10/695,293	MCCLURE, DAVID C.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25,27-30 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25,27-30 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 01/28/05. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-25, 27-30 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Chonan (USP 5463588).

As to claim 1, Chonan discloses in figure 4 a system, comprising: a circuit (the memory circuit and elements, not shown, in circuit 200 that providing signal 250) receiving an enable signal (RAS), the circuit enabled for an operation when the enable signal is in a first state (low) and disabled for that operation when the enable signal is in a second state (column 5, lines 10-28); and a regulator circuit (2) operable responsive to the enable signal to selectively provide a current to the circuit at a first current value when the enable signal is in the first state (when RAS is low that causes Φ2 changes to high, figure 5) and at a second current value when the enable signal is in the second state.

As to claim 2, figure 4 shows that the regulator circuit comprises a plurality of current sources (Q23, Q26 and Q28, Q29).

As to claim 3, figure 4 shows that at least one of the plurality of current sources is selectively activated by an the enable signal.

As to claim 4, figure 4 shows that the plurality of current sources form mirror branches of a current mirror (Q23 and Q29 receive the same bias voltage VERF).

As to claim 5, figure 4 shows that the at least one of the plurality of current sources comprises a first transistor (Q29) and a second transistor (Q28) connected in series to the first transistor, wherein a control terminal of the first transistor is coupled to a control terminal of a transistor (Q23) in a reference leg of the current mirror and a control terminal of the second transistor is coupled to the enable signal.

As to claim 6, figure 4 shows that a delay component (element, not shown, in cirucit 200 that generates signal Φ2) responsive to the enable signal and operable to delay the activation of the at least one of the plurality of current sources relative to the enable signal being in the first state (figure 5 shows that signal Φ2 is a delay of signal RAS).

As to claim 7, figure 4 shows that the delay component is coupled to delay application of the enable signal and the regulator circuit but not the circuit.

As to claim 8, figure 5 shows that the delay component delays one of a rising edge and a falling edge of the enable signal by an amount that is greater than a delay of the other of the rising edge and the falling edge of the enable signal.

As to claim 9, figure 4 shows that the circuit includes a memory device.

As to claim 10, figure 4 shows that the memory device and the regulator circuit both receive an the enable signal, the current value provided by the regulator circuit being based upon a value of the enable signal such that the memory device is enabled for normal operation and

receives the first current value when the enable signal is in the first state and the memory device is disabled from normal operation and receives the second current value when the enable signal is in the second state.

As to claim 11, figure 4 shows a system, comprising: a circuit (the memory circuit and elements, not shown, in circuit 200 that generates signal 250) with an enable signal input and operable for selectively enabling an operation to be performed in the circuit if the enable signal is in a first state and selectively disabling the operation if the enable signal is in the second state (column 5, lines 10-28); and a regulator circuit (2) coupled between a system power source and the circuit and having a control input (gate of Q28) for controlling the amount of supply current available to the circuit, the control input receiving the enable signal and the regulator operating to supply a relatively higher non-zero current level to the circuit when the enable input is in the first state and supply a relatively lower non-zero current level to the circuit when the enable input is in the second state.

As to claim 12, figure 4 shows that the regulator circuit comprises a plurality of current sources (Q23, Q26 and QQ28, Q29), at least one (Q28, Q29) of the plurality of current sources is activated by an the enable signal coupled to the control input of the regulator circuit.

As to claim 13, figure 4 shows that the plurality of current sources form mirror branches of a current mirror.

As to claim 14, figure 4 shows that the at least one of the plurality of current sources (Q28, Q29) is adapted for receiving the enable signal.

As to claim 15, it is inherent that figure 4 has a delay component (elements, not shown, that generates signal Φ2) operable to delay the deactivation of the at least one of the plurality of

current sources relative to the circuit being disabled (figure 5 shows that signal Φ2 is a delay of signal RAS).

As to claim 16, figure 4 shows that the delay component is coupled to delay application of the enable signal and the regulator circuit.

As to claim 17, figure 5 shows that the delay component delays one edge of the enable signal relative to a second edge of the enable signal.

As to claim 18, figure 5 shows that the at least one of the plurality of current sources comprise a first transistor (Q29) and a second transistor (Q28) connected in series to the first transistor, and a control terminal of the second transistor is coupled to the enable signal.

As to claim 19, figure 4 shows that the circuit includes a memory device, and the enable signal input is a chip enable input of the memory device (intended use).

As to claim 20, figure 4 shows that the memory device and the regulator circuit receive the same enable signal.

Claims 21-25, 27-30 and 32 recite a method having similar limitations of claims above. Therefore, they are rejected for the same reasons.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 3, 2005

QUAN TRA
PRIMARY EXAMINER